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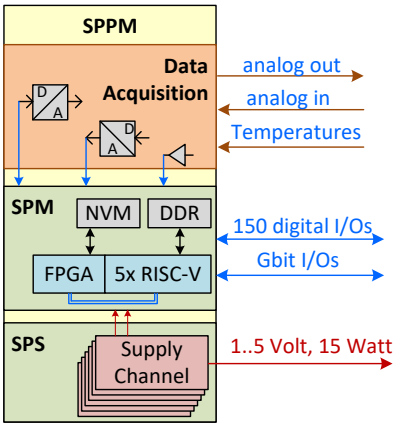
Smart Processing and Power Module (SPPM)

Smart Processing Module (SPM) and Smart Power Supply (SPS).

The Smart Processing and Power Module (SPPM) is a hardware stack of an FPGA-based SoC called the Smart Processing Module (SPM) and its Secondary Power Supply (SPS). Additionally, one or several application boards can be stacked onto the SPM. The development goals have been a certain insensitivity to **radiation loads**, **low power** consumption, and an architecture that supports **serial and parallel data processing**. SPM is a payload controller that supports high data rates and high data throughput applications, such as camera data processing in Earth Observation (EO) missions. Such applications produce data rates on the order of Gbit/s and require processing in orbit as the downlink is usually limited to kbit/s. The processing is performed in real time (i.e., within frame acquisition time) allowing the implementation of algorithms for image processing. Components for the SPM have been selected in one of three ways: a space-qualified counterpart exists (like for PolarFire FPGA), some knowledge about radiation sensitivity is known (from test results), or the technology is intrinsically radiation tolerant (as for MRAM). Total Ionizing Dose radiation tests have demonstrated insensitivity to a level of 20 krad.



Combined with application boards (e.g. a data acquisition board), the SPPM becomes a stand-alone payload computer.

The key features of the SPM, resulting from component selection and/or design, are outlined below.

- **Instant-on behaviour**: The PolarFire SoC, as well as several memory components, are non-volatile, meaning that power cycles do not erase data. The SPM is online millisecond after being powered. The SoC FPGA fabric serves as boot loader for the multicore processor system.
- **Architecture reconfiguration**: Several SoC configurations can be stored in the SPM configuration memory. Thus, the entire SPM can be reconfigured in-orbit.
- **Interfaces and routing**: Almost any communication interface, from SPI to SpaceWire, can be implemented in the SoC, advancing SPM with interface adapter and router features.

The SPS provides for each output two redundant channels that share the electronic load. In case one of the channels fail, the redundant one can overtake. In addition, the power supply protects the SPM and any other payload unit it supplies, against latchups.

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Technical Specifications

FPGA Fabric:

Logic Elements (4-LUT + DFF)	254K
Math Blocks	784
Internal SRAM	17.6 Mbit
SerDes lanes up to 12.7 Gbps	8
Number of Fabirc IOs	372

Microprocessor Subsystem (MSS):

Monitor core	1 × E51 core: RISC-V RV64IMAC, 625 MHz
Application cores	4 × U54 cores; RISC-V RV64GC, 625 MHz
Performance	3.125 CoreMarks/MHz, 1.714 DMIPS/MHz
Interfaces	2 × Gigabit Ethernet MAC; 2 × CAN, 1 × QSPI; 2 × SPI; 2 × I2C; 5 x UART; 1 x USB 2.0 OTG; Additional interfaces can be added as Soft IP in the FPGA Fabric
Number of MSS IOs	136

Power supply and consumption:

MSS+ FPGA power consumption	Min 0.3W (FPGA only), Max 2W
Power supply efficiency	80%
Power supply channels	Adjustable from 1.0 to 5.0 Volt, up to 3 Ampere, latch-up protection with selectable thresholds and trip-off times
Voltage stability	2%
Input Voltage	5-12V

Storage / RAM:

eNVM (Boot Flash)	128 KB
sNVM (secure Boot)	56 KB
MRAM NVM (external connected to Fabric)	16 MB
LPDDR4 (external connected to MSS)	2GB
Mass memory	MMC 5.1 SD/SDIO using microSD card
SPI Flash (Reconfiguration memory)	1Gbit

Connectors:

High-speed inter-board connector	150 digital I/Os, 4 Gbit transceiver lines, power supply
Serial Communication	Micro USB with 4 UART channels
High Speed Transceivers (SerDes)	8x MMCX Connector
Programming	JTAG
Application connectors (optional, to be included into application boards)	MIPI-CSI2.0 camera interface, SpaceWire, USB3.0, Gbit Ethernet, optical fiber communication

Size, Weight:

Length	70 mm
Width	50 mm
Height	20 mm (SPM and SPS, additional height for application boards)
Mass	~180g (SPM and SPS, additional mass for application boards)

Radiation:

Total Ionizing Dose (TiD)	20 kRAD
Single Event Effects (SEE)	SEU protected memories and SEL protected supply

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